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EXPEDITED PROCEDURE - EXAMINING GROUP 2815

S/N 08/903,453 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: George C. Eckert II
Serial No.:	08/903,453	Group Art Unit: 2815
Filed:	July 29, 1997	Docket: 303.378US1
Title:	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS	

SUPPLEMENTAL RESPONSE UNDER 37 C.F.R. § 1.116

Commissioner for Patents
Washington, D.C. 20231

This is a supplemental response to the final Office Action dated 21 June 2002, and is filed with an IDS. The remarks filed on 21 March 2002 and on 23 September 2002 in response to the final Office Action are incorporated herein. The applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 2, 3, 24-28, 41-48, 50-52, and 65-68 are pending in the application, and are rejected. None of the claims have been amended.

Rejection of Claims under §103

Claims 2, 3, 24-28, 41-48, 50-52, and 65-68 were rejected under 35 USC § 103(a) as being unpatentable over Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata), in view of Sugita et al. (JP Patent No. 08-255878, Sugita) and Burns et al., *Principles of Electronic Circuits* , pp. 382-383 (Burns). The applicant respectfully traverses.

Claim 24 recites a transistor comprising a source region in a substrate, a drain region in the substrate, a channel region between the source region and the drain region in the substrate, and a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

Sakata shows in Figure 1 a heterojunction (HJ) diode structure comprising c-Si, a layer of hydrogenated amorphous silicon carbide (a-SiC:H), a layer of hydrogenated amorphous silicon (a-Si:H), another layer of a-SiC:H, and Al. Sakata, page 689, column 1. Sakata is deficient as a reference in that Sakata does not show a source region in a substrate, a drain region in the

substrate, and a channel region between the source region and the drain region in the substrate as are recited in claim 24.

Sugita shows a floating gate transistor with a source and a drain in a substrate, and a polysilicon floating gate separated from the substrate by an insulator.

However, there is no suggestion or motivation to combine Sakata and Sugita.

Sakata states that "the present structure can be used as a component of dynamic random access memories (DRAMs) [4] at room temperature." Sakata, page 689, column 1.

The applicant has submitted a paper entitled *Multi-Day Dynamic Storage of Holes at the AlAs/GaAs Interface* by Qian et al. (Qian) in the IDS filed with this response. Qian shows a p+GaAs/AlAs/n-GaAs capacitor structure in Figure 1 and uses a capacitance-voltage (CV) technique to measure the storage time of holes. Qian, Abstract and Figure 2. In the conclusion Qian notes the CV behavior of the capacitor structure and claims that it is appropriate for use in a dynamic RAM memory device.

Rahman et al., in a paper entitled *Preparation and Electrical Properties of An Amorphous SiC/Crystalline Si p+n Heterostructure*, of record, also analyzes a diode for its CV characteristics.

The applicant notes that Sakata emphasizes the CV characteristics of Sakata's sample diode. Sakata, page 688, column 2. The applicant respectfully submits that Sakata seems to suggest in the text quoted above that the heterojunction structure may be used in a capacitor in a DRAM device.

Sakata also seems to suggest that the heterojunction structure can be used in a floating gate device. The final Office Action emphasizes several quotes from Sakata such as "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Sakata, page 688, column 1. Sakata also says that "heterojunctions on c-Si can be applied to electrically programmable and erasable memory devices." Sakata, abstract.

The final Office Action notes on page 14 Sakata's reference to a paper by Capasso et al. (Capasso) with the sentence "Capasso *et al.* [2] reported similar memory devices based on AlGaAs/GaAs HJ." Sakata, page 688, column 2. Sakata is referring to the earlier statement in the same paragraph, quoted above, that "the HJ structure shown in Fig. 1 can be applied to

floating-gate memory devices." Sakata, page 688, column 1.

Capasso, of record, reports AlGaAs/GaAs floating-gate memory devices. Capasso, abstract. However, Capasso does not show a picture of the device.

The applicant has submitted a paper entitled *Anisotropic Thermionic Emission of Electrons Contained in GaAs/AlAs Floating Gate Device Structures* by Lott et al. (Lott). Lott shows in Figure 1 the mask set and epitaxial layers of a floating gate transistor. Lott refers to the transistor as "[o]ur test vehicle (Fig. 1) has a vertical structure similar to that of Capasso *et al.* " Lott is referring here to the same Capasso paper that Sakata refers to in the quote above from page 688, column 2. The transistor structure shown in Figure 1 of Lott is probably similar to what Sakata is referring to when Sakata says that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Sakata, page 688, column 1. The HJ structure of Sakata may be contemplated by Sakata as being in a floating gate transistor having the same orientation of elements shown in Figure 1 of Lott. This is more likely than the combination of Sakata and Sugita put forward in the final Office Action.

The final Office Action states that the motivation for combining Sakata and Sugita is that "the source, drain and channel regions allow individual floating gate devices to be formed in an array....[t]he use of the source/drain/channel regions for such programming is well known in the art." Final Office Action, page 5. The transistor of Lott has a source, a drain, a gate, and a floating gate. However, the source, drain, and gate shown in Lott are formed next to each other on a superlattice, and the floating gate of Lott is on the other side of the superlattice. A barrier separates the floating gate of Lott from the channel of Lott. The floating gate of Lott is between the source and drain on one side and the channel on the other side, and separates the source and the drain from the channel.

The transistor structure of Lott is substantially different from that of Sugita, even though both have elements with the names source, drain, and floating gate. Sakata and Figure 1 of Lott are linked by their reference to the same paper by Capasso. Lott specifically says that the structure of Figure 1 is similar to that of Capasso. Sakata specifically says that Capasso reported a similar memory device. If there is a suggestion in Sakata for the use of its HJ structure in a floating gate device, it is most probably the floating gate transistor shown by Lott. The

transistors of Lott and Sugita are substantially different, and therefore the applicant respectfully submits that there is no suggestion or motivation to combine Sakata and Sugita.

The structures of the transistors of Sugita and Lott are substantially different, and this is evidence that their principles of operation are different. Sakata refers to the use of Sakata's HJ structure in a floating gate device similar to that shown by Lott, a transistor that probably has a different principle of operation than the transistor of Sugita. Lott is evidence that an addition of elements from Sugita to the HJ diode structure of Sakata would change the principle of operation of Sakata, and therefore the teachings of Sakata and Sugita are not sufficient to render claim 24 *prima facie* obvious.

The applicant respectfully submits that a *prima facie* case of obviousness of claim 24 has **not** been established in the final Office Action, and that claim 24 is in condition for allowance. Claims 25-28 and 44 are dependent on claim 24, and recite further limitations with respect to claim 24. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 25-28 and 44 has **not** been established in the final Office Action, and that claims 25-28 and 44 are in condition for allowance.

Claims 2, 3, 41-43, 45-48, 50-52, and 65-68 recite elements similar to those recited in claim 24. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 2, 3, 41-43, 45-48, 50-52, and 65-68 has **not** been established in the final Office Action, and that claims 2, 3, 41-43, 45-48, 50-52, and 65-68 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 29 October 2002 By _____

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 29th day of October, 2002.

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